Serial No. 09/957,000

**CLAIM AMENDMENTS:**

1. (Previously presented) A method for etching a capacitor structure within a silicon substrate, said method comprising:

providing a masked substrate comprising a patterned masking layer over said silicon substrate, said patterned masking layer having at least one aperture formed therein;

performing a series of process steps upon said silicon substrate through said at least one aperture in said patterned masking layer, said series of process steps comprising (a) an isotropic plasma etching step in which said silicon substrate is etched; and (b) a plasma deposition step in which a passivating layer is deposited on said silicon substrate; and

repeating said series of process steps until a desired etch depth for said capacitor structure is achieved, wherein said capacitor structure comprises an etched sidewall with an undulating profile that has an increased surface area relative to a smooth sidewall.

2. (Original) The method according to claim 1 wherein said capacitor structure ranges from 1-10.0 microns in vertical dimension.

3. (Previously presented) The method according to claim 1, wherein said capacitor structure is a trench structure.

4. (Original) The method according to claim 1 wherein said capacitor structure is an elevated structure.

5-10. (Cancelled)

11. (Previously presented) The method according to claim 1 wherein said isotropic etching step is performed in the presence of a source gas comprising one or more of $SF_6$, $Cl_2$, $NF_3$ and $CF_4$.

12. (Previously presented) The method according to claim 1 wherein said isotropic etching step is performed in the presence of a source gas comprising $SF_6$.

13. (Previously presented) The method according to claim 1 wherein said deposition step is performed in the presence of a source gas comprising a fluorocarbon gas or a fluorohydrocarbon gas.

14. (Previously presented) The method according to claim 1 wherein said deposition step is performed in the presence a source gas comprising of one or more of $C_4F_8$, $CH_2F_2$, $CHF_3$, and $C_4F_6$.

15. (Previously presented) The method according to claim 1 wherein said deposition step is performed in the presence of a source gas comprising $C_4F_8$.

16. (Original) The method according to claim 1 wherein said etching step is conducted at a plasma density ranging from $10^{11}$ to $10^{12}$ $cm^{-3}$.

17. (Original) The method according to claim 1 wherein said etching step proceeds at a rate ranging from 1-3 microns per minute.

18-23. (Cancelled)

24. (Previously presented) The method according to claim 1, wherein said capacitor structure is a trench structure, wherein said isotropic etching step is performed in the presence of a source gas comprising $SF_6$, and wherein said deposition step is performed in the presence of a source gas comprising $C_4F_8$.